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- 1** The sun fireplane system interconnect 87%

Alan Charlesworth  
**Proceedings of the 2001 ACM/IEEE conference on Supercomputing (CDROM)**  
November 2001

System interconnect is a key determiner of the cost, performance, and reliability of large cache-coherent, shared-memory multiprocessors. Interconnect implementations have to accommodate ever greater numbers of ever faster processors. This paper describes the Sun™ Fireplane two-level cache-coherency protocol, and its use in the medium and large-sized UltraSPARC-III-based Sun Fire™ servers.
- 2** Performance analysis using the MIPS R10000 performance counters 84%

Marco Zagha , Brond Larson , Steve Turner , Marty Itzkowitz  
**Proceedings of the 1996 ACM/IEEE conference on Supercomputing (CDROM)**  
November 1996

Tuning supercomputer application performance often requires analyzing the interaction of the application and the underlying architecture. In this paper, we describe support in the MIPS R10000 for non-intrusively monitoring a variety of processor events -- support that is particularly useful for characterizing the dynamic behavior of multi-level memory hierarchies, hardware-based cache coherence, and speculative execution. We first explain how performance data is collected using an integrate ...
- 3** A write update cache coherence protocol for min-based multiprocessors 82%